Capacitor pipeline

Can capacitor and opamp sharing improve low power pipeline ADC design?
Abstract-- A new capacitor and opamp sharing technique that enables a very efficient low power pipeline ADC design is proposed. A new method to cancel the effect of signal-dependent kick-back in the absence of sample and hold is also presented.

Do I need a weighted capacitor array to calibrate a pipeline ADC?
Although the analog calibration does not require extra clock cycles during normal conversions,a weighted capacitor array is neededfor each stage to be calibrated. For pipeline ADC'S,where many stages are calibrated,the added complexity and capacitive load is significant.

Why should capacitor size and opamp design/bias be scaled?
Because the accuracy requirements gradually decrease to the later stages of the pipeline architecture,properly scaling the capacitor size and opamp design/bias can efficiently reduce power consumptionwhile maintaining the same ADC resolution .

Can a capacitor share reduce opamp load?
To reduce power in it,a capacitor sharing technique was recently proposed ,where the residue held on the feedback capacitor is used for the next stage MDAC operation thereby reducing the opamp load. This means that every alternate stage in the ADC can be made load-free.

Is capacitor sharing a suitable partner for opamp sharing?
Capacitor sharing is found to be a suitable partner for opamp sharing. A new method to cancel the effect of signal-dependent charge kick-back in the absence of sample and hold was also presented. This was achieved via capacitor swapping to neutralize/reset the charge in the input capacitors between samples.

Can a digital self-calibration technique be used for pipeline ADCs?
For pipeline ADC'S, where many stages are calibrated, the added complexity and capacitive load is significant. This paper presents a digital self-calibration technique based on a radix 1.93 and one comparator per stage conversion algorithm. A nonradix two conversion algorithm was previ-ously employed in a successive approximation converter .

In this paper we present a simple charge-sharing solution, by pre-charging the load capacitors properly, the initial input voltage step is minimized. The technique is simulated in a SC pipeline residue amplifier, and it provides 5.4 dB (nearly 1 bit) improvement in the settling accuracy with no additional active components.

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Capacitor pipeline

The invention relates to switched-capacitor circuits for analog-to-digital converters (ADCs) having a pipeline architecture, and in particular to circuit designs allowing for both reference and...

This work presents a low-power 10-bit 40 MSPS Pipelined ADC with 1.8V supply voltage in a 180nm silicon-based CMOS process. Simultaneous capacitor sharing and ...

This work presents a low-power 10-bit 40 MSPS Pipelined ADC with 1.8V supply voltage in a 180nm silicon-based CMOS process. Simultaneous capacitor sharing and op-amp sharing technique is used between two successive stages of a Sample-and-Hold Amplifier (SHA) to reduce the power consumption.

The proposed architecture exhibits lower sensitivity to jitter when compared to the conventional switched-capacitor pipeline ADC. This continuous-time input architecture has been enabled by the introduction of low precision signal prediction within the ADC CT input first stage.

SC pipeline architecture is used followed by an output driver. For GHz frequency operation with output voltage swing suitable for wireless applications (300 mVpp) the DAC performance is ...

A new pipeline ADC architecture that employs a continuous-time first stage followed by a conventional switched capacitor pipeline ADC is presented. Such an approach overcomes many of the challenges associated with a pure switched-capacitor architecture and leads to a low area, low power solution with excellent distortion performance.

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consumption of analog designs generally increases with reduced supply voltage. Recently, with the demand for longer battery life in mobile systems, low power pipeline ADC is highly attractive. Therefore, in this project, our primary goal was to find a power-efficient pipeline ADC architecture to reduce the power consumption.

Senior Member, Abstract-A 15-b l-Msample/s digitally self-calibrated pipeline analog-to-digital converter (ADC) is presented. A radix 1.93, 1 b per stage design is employed. The digital self-calibration accounts for capacitor mismatch, comparator offset, charge injection, finite op-amp gain, and capacitor nonlinearity contributing to DNL.

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